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Search Results -

Terms	Documents
(program$5 adj cell$1) same process$3	508

Database: US Patents Full-Text Database

Refine Search: (program$5 adj cell$1) same process$3

Search History

DB Name	Query	Hit Count	Set Name
USPT	(program$5 adj cell$1) same process$3	508	L1

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Search Results -

Terms	Documents
(program$5 adj cell$1) same process$3	6

Database: JPO Abstracts Database

Refine Search: (program$5 adj cell$1) same process$3

Search History

DB Name	Query	Hit Count	Set Name
JPAB	(program$5 adj cell$1) same process$3	6	L2
USPT	(program$5 adj cell$1) same process$3	508	L1

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Search Results -

Terms	Documents
(program$5 adj cell$1) same process$3	29

Database: EPO Abstracts Database

Refine Search: (program$5 adj cell$1) same process$3

Search History

DB Name	Query	Hit Count	Set Name
EPAB	(program$5 adj cell$1) same process$3	29	L3
JPAB	(program$5 adj cell$1) same process$3	6	L2
USPT	(program$5 adj cell$1) same process$3	508	L1

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Search Results -

Terms	Documents
l1 and ((program$5 adj cell$1) same process$3)	15

Database: US Patents Full-Text Database

Refine Search:

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l1 and ((program$5 adj cell$1) same
process$3)
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Search History

DB Name	Query	Hit Count	Set Name
USPT	l1 and ((program$5 adj cell$1) same process$3)	15	L2
USPT	710/100.ccls. or 710/129.ccls. or 712/11.ccls. or 712/14.ccls. or 712/18.ccls. or 712/25.ccls. or 712/29.ccls. or 711/100.ccls. or 326/38.ccls. or 326/39.ccls. or 326/41.ccls. or 364/489.ccls. or 370/419.ccls. or 710/110.ccls. or 712/31.ccls.	3415	L1

Document Number 2

Entry 2 of 15 File: USPT Aug 10, 1999

US-PAT-NO: 5937202
DOCUMENT-IDENTIFIER: US 5937202 A

TITLE: High-speed, parallel, processor architecture for front-end electronics, based on a single type of ASIC, and method use thereof

DATE-ISSUED: August 10, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Crosetto; Dario B.	DeSoto	TX	N/A	N/A

US-CL-CURRENT: 712/19; 712/11

ABSTRACT:

An array of processors, each having a data input for receiving raw data, and other data input ports for receiving data for other processors of the plurality. Each processor processes data according to an algorithm programmed therein, and either passes the processed data or raw data to the other processors. By using a three dimensional array of processors, data from a large number of inputs can be processed in a high speed manner and funneled to a smaller number of outputs. An efficient microcode and processor architecture allows high speed processing of data using very few clock cycles, and can pass raw data to another processor in a single clock cycle.
39 Claims, 97 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 79

Document Number 4

Entry 4 of 15 File: USPT Aug 20, 1996

US-PAT-NO: 5548773
DOCUMENT-IDENTIFIER: US 5548773 A

TITLE: Digital parallel processor array for optimum path planning

DATE-ISSUED: August 20, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kemeny; Sabrina E.	La Crescenta	CA	N/A	N/A
Fossum; Eric R.	La Crescenta	CA	N/A	N/A
Nixon; Robert H.	Shadow Hills	CA	N/A	N/A

US-CL-CURRENT: 712/11; 364/DIG1, 364/DIG2, 701/200, 701/201, 705/400

ABSTRACT:

The invention computes the optimum path across a terrain or topology represented by an array of parallel processor cells interconnected between neighboring cells by links extending along different directions to the neighboring cells. Such an array is preferably implemented as a high-speed integrated circuit. The computation of the optimum path is accomplished by, in each cell, receiving stimulus signals from neighboring cells along corresponding directions, determining and storing the identity of a direction along which the first stimulus signal is received, broadcasting a subsequent stimulus signal to the neighboring cells after a predetermined delay time, whereby stimulus signals propagate throughout the array from a starting one of the cells. After propagation of the stimulus signals throughout the array, a master processor traces back from a selected destination cell to the starting cell along an optimum path of the cells in accordance with the identity of the directions stored in each of the cells.
56 Claims, 9 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 7

Document Number 8

Entry 8 of 15 File: USPT May 30, 1995

US-PAT-NO: 5421019
DOCUMENT-IDENTIFIER: US 5421019 A

TITLE: Parallel data processor

DATE-ISSUED: May 30, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holsztynski; Wlodzimierz	Mountainview	CA	N/A	N/A
Benton; Richard W.	Altamonte Springs	FL	N/A	N/A
Johnson; W. Keith	Goleta	CA	N/A	N/A
McNamara; Robert A.	Orlando	FL	N/A	N/A
Naeyaert; Roger S.	Plano	TX	N/A	N/A
Noden; Douglas A.	Orlando	FL	N/A	N/A
Schoomaker; Ronald W.	Orlando	FL	N/A	N/A

US-CL-CURRENT: 712/14; 364/229.4, 364/231.9, 364/239.51, 364/246.3, 364/DIG1, 712/22

ABSTRACT:

A parallel data processor comprised of an array of identical cells concurrently performing identical operations under the direction of a central controller, and incorporating one or more of a special cell architecture including a segmented memory, conditional logic for preliminary processing, and circuitry for indicating when the cell is active, and programmable cell interconnection including cell bypass and alternate connection of edge cells.
43 Claims, 10 Drawing figures
Exemplary Claim Number: 23
Number of Drawing Sheets: 9

Document Number 9

Entry 9 of 15 File: USPT May 23, 1995

US-PAT-NO: 5418952
DOCUMENT-IDENTIFIER: US 5418952 A

TITLE: Parallel processor cell computer system

DATE-ISSUED: May 23, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Morley; Richard E.	Mason	NH	N/A	N/A
Currie, Jr.; Douglas H.	Londonderry	NH	N/A	N/A
Szakacs; Gabor L.	Nashua	NH	N/A	N/A

US-CL-CURRENT: 712/14; 364/229, 364/229.2, 364/230.1, 364/230.3, 364/231.9, 364/232.1 , 364/280.7, 364/281.3, 364/281.4, 364/DIG1, 712/20

ABSTRACT:

A computer system especially for solution of real time inference problems is disclosed. The system includes a systolic cellular processor which provides predictable and responsive real time operation and fine grain programmability. The system comprises a plurality of separate processor cells each having its own local memory, the cells running simultaneously and operative to execute their respective program instructions. A global memory is coupled via a global bus to the processor cells and provides data to the cells and stores data from the cells. The bus provides effectively simultaneous access of all cells to the global memory. A further feature of the system is a novel parallel programming language using English syntax and which provides synchronous and predictable binding of code to each cell. A graphic work station is provided as a user interface to provide visual access to each cell or to cell groups for ease of control. The system can also function to emulate large scale integrated circuit processors by reason of the fine grain programmed operation of the system.
12 Claims, 24 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 13

Document Number 12

Entry 12 of 15 File: USPT Jan 23, 1990

US-PAT-NO: 4896296
DOCUMENT-IDENTIFIER: US 4896296 A

TITLE: Programmable logic device configurable input/output cell

DATE-ISSUED: January 23, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Turner; John E.	Beaverton	OR	N/A	N/A
Rutledge; David L.	Beaverton	OR	N/A	N/A
Darling; Roy D.	Forest Grove	OR	N/A	N/A

US-CL-CURRENT: 326/38; 340/825.83, 365/189.08, 708/230

ABSTRACT:

An in-system programmable logic device is disclosed which may be configured or reconfigured while installed in a user's system. The disclosed device employs non-volatile memory cells such as floating gate transistors as the programmable elements, and hence the device retains a particular programmed logic configuration virtually indefinitely during a powered-down state. The device is operable in a normal state and in several utility states for reconfiguring the device. The device state is controlled by an internal state machine which executes several state equations whose variables are the logic levels driving two dedicated pins and the present device state. One device pin receives serial input data which loads a shift register latch. The contents of the latch are employed to select a particular row of the cells to be programmed and the logic level to which the selected cells are to be programmed. The device normal inputs and outputs are isolated from the device during the utility states, so that the user's system does not affect the device operation during the utility states. A voltage multiplier circuit is included to generate the high voltage level necessary to program the floating gate transistors employed as the device memory cells from the device supply voltage, thereby further conserving on the required number of device pins. By programming a particular memory cell, the user may select the state of the device outputs during the utility states as either a present data latched condition or a tri-stated condition.
14 Claims, 42 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 24

Document Number 14

Entry 14 of 15 File: USPT Aug 8, 1989

US-PAT-NO: 4855954
DOCUMENT-IDENTIFIER: US 4855954 A

TITLE: In-system programmable logic device with four dedicated terminals

DATE-ISSUED: August 8, 1989

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Turner; John E.	Beaverton	OR	N/A	N/A
Rutledge; David L.	Beaverton	OR	N/A	N/A
Darling; Roy D.	Forest Grove	OR	N/A	N/A

US-CL-CURRENT: 326/39; 326/88, 365/185.01, 365/185.17, 365/189.08, 365/200, 365/233, 708/230

ABSTRACT:

An in-system programmable logic device is disclosed which may be configured or reconfigured while installed in a user's system. The disclosed device employs non-volatile memory cells such as floating gate transistors as the programmable elements, and hence the device retain a particular programmed logic configuration virtually indefinitely during a powered-down state. The device is operable in a normal state and in several utility states for reconfiguring the device. The device state is controlled by an internal state machine which executes several state equations whose variables are the logic levels driving two dedicated pins and the present device state. One device pin receives serial input data which loads a shift register latch. The contents of the latch are employed to select a particular row of the cells to be programmed and the logic level to which the selected cells are to be programmed. The device normal inputs and outputs are isolated from the device during the utility states, so that the user's system does not affect the device operation during the utility states. A voltage multiplier circuit is included to generate the high voltage level necessary to program the floating gate transistors employed as the device memory cells from the device supply voltage, thereby further conserving on the required number of device pins. By programming a particular memory cell, the user may select the state of the device outputs during the utility states as either a present data latched condition or a tri-stated condition.
4 Claims, 59 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 22

Document Number 15

Entry 15 of 15 File: USPT

US-PAT-NO: 4251861
DOCUMENT-IDENTIFIER: US 4251861 A

TITLE: Cellular network of processors

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Mago; Gyula A.	Chapel Hill	NC	27514	N/A

US-CL-CURRENT: 712/18

ABSTRACT:

A network of processors having a cellular structure is capable of directly and efficiently executing a predetermined class of programing languages such as applicative languages. The network includes two interconnected networks of processors, one of which is a linear array of cells of a first kind and the other a tree network of cells of a second kind. The network directly interprets a high level language and is capable of operating on a wide range of classes of programs. Within practical limits, the network accommodates the unbounded parallelism permitted by applicative languages in a single user program. The network also has the capability of executing many user programs simultaneously.
26 Claims, 44 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 21

Document Number 1

Entry 1 of 1 File: EPAB Aug 13, 1998

PUB-NO: WO009835299A2
DOCUMENT-IDENTIFIER: WO 9835299 A2
TITLE: METHOD FOR SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE COMPONENT
PUBN-DATE: August 13, 1998

INVENTOR-INFORMATION:

NAME	COUNTRY
VORBACH, MARTIN	DE
MUENCH, ROBERT	DE

INT-CL (IPC): G06 F 15/78

EUR-CL (EPC): G06F015/78

ABSTRACT:

The invention relates to a method for synchronization and reconfiguration of configurable elements in components with two-dimensional or multidimensional programmable cell structure (DFP, FPGA, DPGA, RAW machine) as well as to the control of conditioned branches in common microprocessors, digital signal processors and microcontrollers. According to said method, synchronization signals are generated during processing within the data flow by the elements that are to be processed and configured by means of comparisons, algebraic signs, transmission of arithmetic operations, error status or the like, and are sent to additional elements for synchronization via the data bus. Configuration words within a configurable element are generated from the data flow on the basis of corresponding commands and communicated, along with the address of the register to be picked up, to a further configurable element via the data bus, wherein said element is thus (re)configured without the influence of an external load logic. A valid configuration of the configurable elements from a plurality of configurations or a valid command from multiple possible commands of an arithmetic processing unit is then selected during running time on the basis of synchronization signals.

Document Number 1

Entry 1 of 6 File: JPAB Sep 9, 1994

PUB-NO: JP406251592A
DOCUMENT-IDENTIFIER: JP 06251592 A
TITLE: METHOD AND DEVICE FOR PREVENTING EXCESSIVE ERASE OF FLASH CELL

PUBN-DATE: September 9, 1994

INVENTOR-INFORMATION:
NAME
TURNER, JOHN E

INT-CL (IPC): G11C 16/06; H03K 19/173; H03K 19/177

ABSTRACT:

PURPOSE: To prevent excessive erase of a flash cell.

CONSTITUTION: A flash cell 10 consists of a gate 11, a source 12, a drain 14, and a floating gate 17. The gate and the source of this programmed cell 10 are grounded, and a high voltage 16 is applied to the drain through a high impedance element. Thus, electric charge on the floating gate is removed through the drain and the high impedance element. Since most of the high voltage is dropped by the high impedance element at the same time that the cell enters a depletion start point to start being conductive, the voltage applied to the floating gate is not enough to keep a Fowell-Nordheim tunnel, and erase processing is self-stopped.

Document Number 2

Entry 2 of 6 File: JPAB Aug 5, 1992

PUB-NO: JP404214298A
DOCUMENT-IDENTIFIER: JP 04214298 A
TITLE: PROGRAMMING METHOD FOR PROGRAMMABLE ELEMENT IN PROGRAMMABLE DEVICE

PUBN-DATE: August 5, 1992

INVENTOR-INFORMATION:
NAME
NORMAN, KEVIN A
SANSBURY, JAMES D
HERRMANN, ALAN L
HENDRICKS, MATTHEW C
NOUBAN, BEHZAD

INT-CL (IPC): G11C 16/06

ABSTRACT:

PURPOSE: To quicken the programming of a programmable logic device(PLD), also to perform the programming with the highest program possible voltage and also to reduce the number of unsuccessful devices.

CONSTITUTION: As high voltage pulse impressing processes programming the EPROM cell in a PLD, a first path in which a pulse is the pulse of 200μs and whose number of maximum settings is 20 pieces, a second path in which a pulse is the pulse of 50μs and whose number of maximum settings is 80 pieces and a third path in which a pulse is the pulse of 20μs and whose number of maximum settings is 100 pieces are provided. At first, a threshold value voltage is verfied every one pulse impression with respect to a cell with the first path and when the threshold voltage reaches a program voltage, after impressing the impressed number of pulses as excessive pulses again and the programming of another cell is performed. When the threshold voltage does not reach the program voltage even after the impression of 20 pieces of pulse, after pulses of the number of the maximum number are impressed again, the path is moved to the second path and the same pulse impression is performed. This pulse impressing method is repeated till the third path.

Document Number 3

Entry 3 of 6 File: JPAB Jan 11, 1990

PUB-NO: JP402007297A
DOCUMENT-IDENTIFIER: JP 02007297 A
TITLE: CIRCUIT FEEDING LOAD FOR CHARGING ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY CELL

PUBN-DATE: January 11, 1990

INVENTOR-INFORMATION:
NAME
JUNGROTH, OWEN W

INT-CL (IPC): G11C 16/06

ABSTRACT:

PURPOSE: To obtain a load line used at the time of programing an EPROM cell by combining the gate of a third and fourth transistor to a circuit point between a first transistor and a second matched transistor and feeding a load for charging a reading only memory cell.

CONSTITUTION: When a drain terminal is made to be a positive potential in order to program a cell 24, an electric charge is injected into the gate from a chanel and a drain area should be kept at about 6. 5 V during this injecting operation. A hot electron is stopped to inject at the time of the voltage drop far lower than 6V, and the cell is not programed. On the other hand, when the drain voltage exceeds 7V, the other memory cells connected to a line 42 being programed are disturbed, whereby some potential of those memory cells are lost. And the variation of the load line, due to the change of threshold voltage relating to the variation of manufacturing process and the change of temperature, is largely reduced. By this way, a desired potential is fed to the circuit point in order to program cells.

Document Number 4

Entry 4 of 6 File: JPAB Mar 27, 1990

PUB-NO: JP402086325A
DOCUMENT-IDENTIFIER: JP 02086325 A
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT

PUBN-DATE: March 27, 1990

INVENTOR-INFORMATION:
NAME
SAITO, HITOSHI

INT-CL (IPC): H03K 19/177; G06F 7/00

ABSTRACT:

PURPOSE: To take a readout inhibit processing independently of a diode while disabling a decoder function by providing a 2-input NOR circuit to an input address of an input buffer and writing a security bit in a security bit program cell.

CONSTITUTION: An X address buffer 11 consists of an inverter 11a and part of a 2-input NOR circuit 11b. A security bit program cell Q3 acts like a diode equivalently by writing a security bit thereto to keep a security data SEC' at an input point of a security output buffer 14a to an L level. Thus, an X decoder function is disabled to attain the readout inhibit processing.

Document Number 5

Entry 5 of 6 File: JPAB Feb 19, 1988

PUB-NO: JP363039037A
DOCUMENT-IDENTIFIER: JP 63039037 A
TITLE: PROGRAM CALL PROCESSING SYSTEM

PUBN-DATE: February 19, 1988

INVENTOR-INFORMATION:
NAME
KOZAMA, TOSHIYUKI

INT-CL (IPC): G06F 9/44; G06F 9/44

ABSTRACT:

PURPOSE: To increase the processing speed of a compiler which is executed by an interpreter by providing the different intermediate texts according to the type of the program of the called side for a program cell instruction and obtaining a storing place address of the program directly from the operand of the intermediate text.

CONSTITUTION: When the subroutine of an interpreter is called, the operand address of an intermediate text is immediately carried out at a process stage 41 through the entrance address of a subroutine designated as a relative address. When the module of a compiler is called, an intermediate module refers to a call module table 50 at a process state 43 and starts the execution of a loaded module as long as a module item is designated. While a single item is set to a module table 50 if no call is given. Then an access is started to a designated module with a file number designated by the operand of the intermediate text.

Document Number 6

Entry 6 of 6 File: JPAB Jul 7, 1982

PUB-NO: JP357109176A
DOCUMENT-IDENTIFIER: JP 57109176 A
TITLE: LIST PROCESSING SYSTEM

PUBN-DATE: July 7, 1982

INVENTOR-INFORMATION:
NAME
HIROSE, SADAKI
SHINOKI, TAKESHI

INT-CL (IPC): G11C 9/06; G06F 9/44; G06F 13/00

ABSTRACT:

PURPOSE: To enable the scattering of program interruption at list processing for a long time, by providing two mark bits for each cell and using them for marking, correcting processing in garbage correction.

CONSTITUTION: When a new cell is used, two sets of mark bits are set to a flag register FLG, another mark bit of the cell coming from the specified element of a stack area SP is inverted for marking. Correcting processing is made with the mark bit, the first cell pointer not marked is set to a control pointer CP for sub- marking and sub-correcting. Thus, while the processing program does not use all the cells, if cells are newly used, gabbage correction can be made with scattering. As a result, the program interruption for a long time by the garbage correction is scattered and one intermittent time is decreased, resulting in list processing system effective for real time processing.

Document Number 2

Entry 2 of 24 File: USPT May 25, 1999

US-PAT-NO: 5907855
DOCUMENT-IDENTIFIER: US 5907855 A

TITLE: Apparatus and method for reducing programming cycles for multistate memory system

DATE-ISSUED: May 25, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Norman; Robert D.	San Jose	CA	N/A	N/A

US-CL-CURRENT: 711/103; 365/185.22, 365/189.01, 365/189.11, 365/45, 711/100, 711/205

ABSTRACT:

An apparatus and method for reducing the number of programming states (threshold voltage levels) required to be traversed when programming a multistate memory cell with a given set of data. The invention first determines the average programming state (corresponding to an average threshold voltage level) for the set of data which is to be programmed into the memory cells. This is accomplished by counting the number of programming states which must be traversed in programming the cells with the data. If the majority of the data requires programming the memory cell(s) to the upper two programming states (in the case of a two bit per cell or four state system), then the data is inverted and stored in the memory in the inverted form. This reduces the amount of programming time, the number of programming states traversed, and the power consumed in programming the memory cell(s) with the data field. In the case of data which is encoded using a scheme other than a direct sequential ordering of the threshold voltage levels, the encoded data is converted into an alternate form prior to counting the states. A flag indicating the translation operation (inversion of states, reassignment of states to different levels, etc.) used to assign the existing threshold voltage levels to those that will be programmed into the memory cells is also stored. The flag can be used to indicate the transformation process needed to convert the stored data back to its original form.
19 Claims, 12 Drawing figures
Exemplary Claim Number: 17
Number of Drawing Sheets: 12

Document Number 11

Entry 11 of 24 File: USPT May 30, 1995

US-PAT-NO: 5421019
DOCUMENT-IDENTIFIER: US 5421019 A

TITLE: Parallel data processor

DATE-ISSUED: May 30, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holsztynski; Wlodzimierz	Mountainview	CA	N/A	N/A
Benton; Richard W.	Altamonte Springs	FL	N/A	N/A
Johnson; W. Keith	Goleta	CA	N/A	N/A
McNamara; Robert A.	Orlando	FL	N/A	N/A
Naeyaert; Roger S.	Plano	TX	N/A	N/A
Noden; Douglas A.	Orlando	FL	N/A	N/A
Schoomaker; Ronald W.	Orlando	FL	N/A	N/A

US-CL-CURRENT: 712/14; 364/229.4, 364/231.9, 364/239.51, 364/246.3, 364/DIG1, 712/22

ABSTRACT:

A parallel data processor comprised of an array of identical cells concurrently performing identical operations under the direction of a central controller, and incorporating one or more of a special cell architecture including a segmented memory, conditional logic for preliminary processing, and circuitry for indicating when the cell is active, and programmable cell interconnection including cell bypass and alternate connection of edge cells.
43 Claims, 10 Drawing figures
Exemplary Claim Number: 23
Number of Drawing Sheets: 9

Document Number 16

Entry 16 of 24 File: USPT Jan 12, 1993

US-PAT-NO: 5179714
DOCUMENT-IDENTIFIER: US 5179714 A

TITLE: Parallel bit serial data processor

DATE-ISSUED: January 12, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Graybill; Robert B.	Ellicott City	MD	N/A	N/A

US-CL-CURRENT: 712/19; 364/229.2, 364/231.9, 364/238, 364/238.3, 364/247, 364/247.3, 364/258, 364/258.1, 364/DIG1

ABSTRACT:

A single instruction multiple data systolic array processor having provision for local address generation, direct access to external devices, and programmable cell interconnectivity for providing great versatility while at the same time retaining the advantages of the SIMD architecture.
3 Claims, 13 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 12

Document Number 17

Entry 17 of 24 File: USPT

US-PAT-NO: 5113498
DOCUMENT-IDENTIFIER: US 5113498 A

TITLE: Input/output section for an intelligent cell which provides sensing, bidirectional communications and control

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Evan; Shabtai	Saratoga	CA	N/A	N/A
Sander; Wendell B.	Los Gatos	CA	N/A	N/A

US-CL-CURRENT: 710/8; 364/221, 364/221.1, 364/228, 364/228.1, 364/231.8, 364/232.2, 364/232.8, 364/237.8, 364/238.3, 364/240, 364/240.8, 364/240.9, 364/241.9, 364/242.94, 364/242.96, 364/244, 364/244.3, 364/244.6, 364/244.9, 364/247, 364/247.2, 364/247.5, 364/247.6, 364/247.7, 364/247.8, 364/254, 364/254.5, 364/259, 364/259.1, 364/259.3, 364/259.5, 364/260, 364/260.3, 364/260.4, 364/260.81, 364/262, 364/262.3, 364/262.4, 364/262.9, 364/270, 364/271, 364/271.4, 364/271.5, 364/281.3, 364/284, 364/284.3, 364/284.4, 364/DIG1

ABSTRACT:

A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a processor and input/output section are coupled to the network. Each of the programmable cells receives when manufactured a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power lines, twisted, pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network. The preferred embodiment of the cell includes a multiprocessor and multiple I/O subsections where any of the processors can communicate with any of the I/O subsections. This permits the continual execution of a program without potential interruptions caused by interfacing with the I/O section. The I/O section includes programmable A-to-D and programmable D-to-A converters as well as other circuits for other modes of operation.
21 Claims, 30 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 18

Document Number 20

Entry 20 of 24 File: USPT Feb 12, 1985

US-PAT-NO: 4499557
DOCUMENT-IDENTIFIER: US 4499557 A

TITLE: Programmable cell for use in programmable electronic arrays

DATE-ISSUED: February 12, 1985

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Holmberg; Scott H.	Milford	MI	N/A	N/A
Flasck; Richard A.	Rochester	MI	N/A	N/A

US-CL-CURRENT: 365/163; 257/368, 257/480, 257/754, 257/769, 257/926, 365/174

ABSTRACT:

An improved programmable cell for use in programmable electronic arrays such as PROM devices, logic arrays, gate arrays and die interconnect arrays. The cells have a highly non-conductive state settable and non-resettable into a highly conductive state. The cells have a resistance of 10,000 ohms or more in the non-conductive state which are settable into the conductive state by a threshold voltage of 10 volts or less, a current of 25 milliamps or less, for 100 microseconds or less. The cells in the conductive state have a resistance of 100 ohms or less. The cells have a maximum permittable processing temperature of 400.degree. centigrade or more and a storage temperature of 175.degree. centigrade or more. The cells are formed from doped silicon alloys including at least hydrogen and/or fluorine and contain from about 0.1 to 5 percent dopant. The cells can be plasma deposited from silane or silicon tetrafluoride and hydrogen with 20 to 150,000 ppm of dopant.

Each cell in an array is a thin film deposited cell and includes an isolating device which can be a bipolar or MOS device or can be a thin film diode or transistor. The associated addressing circuitry also can be conventional bipolar or MOS devices or thin film deposited devices. The cells have a cell area of less than one square mil to provide a high cell packing density.
37 Claims, 16 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 6